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	Application No.	Applicant(s)	
Mating of Allowskiller	10/642,737	KARASAWA ET AL.	
Notice of Allowability	Examiner	Art Unit	
	Pamela E. Perkins	2822	
The MAILING DATE of this communication appe All claims being allowable, PROSECUTION ON THE MERITS IS herewith (or previously mailed), a Notice of Allowance (PTOL-85) NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RI of the Office or upon petition by the applicant. See 37 CFR 1.313	(OR REMAINS) CLOSED in this ap or other appropriate communication GHTS. This application is subject t	pplication. If not included n will be mailed in due cours	
1. \boxtimes This communication is responsive to <u>the amendment filed or</u>	on 29 July 2005.		
2. X The allowed claim(s) is/are <u>1-57</u> .			
3. \boxtimes The drawings filed on <u>19 May 2004</u> are accepted by the Ex	aminer.		
4.	been received. been received in Application No cuments have been received in this of this communication to file a reply ENT of this application. itted. Note the attached EXAMINER as reason(s) why the oath or declara to be submitted. on's Patent Drawing Review (PTO- as Amendment / Comment or in the Comment or i	national stage application from the requirement of	nents E OF
 Attachment(s) 1. ☐ Notice of References Cited (PTO-892) 2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948) 3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/05 Paper No./Mail Date 6/24/05 4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material 	6. ☐ Interview Summary Paper No./Mail Da 8), 7. ☐ Examiner's Amenda	te	,

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DETAILED ACTION

This office action is in response to the filing of the amendment on 7 July 2005.

Claims 1-57 are pending; claims 58 and 59 have been canceled.

Allowable Subject Matter

Claims 1-57 are allowed.

Reasons for Allowance

The following is an examiner's statement of reasons for allowance: prior art does not anticipate, teach, or suggest a method of manufacturing a semiconductor device where a protrusion is formed on a semiconductor substrate having a first area and a second area surrounding the first area, the protrusion protruding above the first area; disposing a support on a surface of the semiconductor substrate on which the protrusion is formed, so that a through hole of the support overlaps with the first area and the protrusion is set in an opening of the through hole; and grinding the semiconductor substrate from a surface opposite to the surface on which the protrusion is formed.

For example, Ohuchi et al. (6,353,267) disclose a method of manufacturing a semiconductor device where a protrusion is formed on a semiconductor substrate having a first area, the protrusion protruding above the first area; disposing a resin layer on a first area of a semiconductor substrate; disposing a through hole overlapping the first area; and grinding the semiconductor substrate from a surface opposite to the

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surface on which the protrusion is formed. However, Ohuchi et al. do not disclose, anticipate, teach, or suggest forming at least one protrusion in a through hole.

Sahara et al. (6,713,880) disclose a method of manufacturing a semiconductor device where a protrusion is formed on a semiconductor substrate having a first area and a second area surrounding the first area, the protrusion protruding above the first area; disposing a resin layer on a first area of the semiconductor substrate; and disposing a support on a surface of the semiconductor substrate on which the protrusion is formed, a part of the support overlapping with the second area being thicker than another part of the support overlapping with the first area. However, Sahara et al. do not disclose, anticipate, teach or suggest forming at least one protrusion in a through hole.

The prior art made of record in this action does not anticipate, teach, or suggest a method of manufacturing a semiconductor device where a protrusion is formed on a semiconductor substrate having a first area and a second area surrounding the first area, the protrusion protruding above the first area; disposing a support on a surface of the semiconductor substrate on which the protrusion is formed, so that a through hole of the support overlaps with the first area and the protrusion is set in an opening of the through hole; and grinding the semiconductor substrate from a surface opposite to the surface on which the protrusion is formed.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably Application/Control Number: 10/642,737

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accompany the issue fee. Such submissions should be clearly labeled "Comments on

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Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Pamela E. Perkins whose telephone number is (571)

272-1840. The examiner can normally be reached on Monday thru Friday, 8:30am to

5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number

for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

PEP

Michael Trinh Primary Examiner

Jullis

Act SPE